circuit arrangements and/or implementations for the voltage sources, as desired. For example, one may use voltage references described in U.S. Patent Application Serial No. 10/081,121, Attorney Docket No. SILA:095, titled "Calibrated Low-Noise Current and Voltage References and Associated Methods," as desired.

In the Claims:

Claim 1 is being amended.

Please cancel claim 2.

Please add new claims 3-43.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).

1. A calibration circuitry, comprising:

an adjustable capacitor, the adjustable capacitor having a capacitance that varies in response to a plurality of control signals;

a voltage generator, the voltage generator configured to provide a measurement voltage that depends on the capacitance of the adjustable capacitor;

a reference voltage generator, the reference voltage generator configured to provide a reference voltage; and

a controller, the controller configured to provide the plurality of control signals based on the relative values of the reference voltage and the measurement voltage.

3. The calibration circuitry according to claim 1, wherein the measurement voltage is generated by alternately charging and discharging the adjustable capacitor.

4. The calibration circuitry according to claim 3, wherein the adjustable capacitor is calibrated by holding the plurality of control signals constant after powering up the calibration circuitry.

5. The calibration circuitry according to claim 4, wherein the adjustable capacitor is charged in response to a first clock signal.

6. The calibration circuitry according to claim 5, wherein the adjustable capacitor is discharged in response to a second clock signal.

7. The calibration circuitry according to claim 6, wherein the first and second clock signals are non-overlapping.

8. The calibration circuitry according to claim 7, wherein the controller comprises a logic circuitry.

9. The calibration circuitry according to claim 8, wherein the logic circuitry comprises a finite-state machine configured to provide the plurality of control signals.

10. The calibration circuitry according to claim 9, wherein the finite-state machine uses successive approximation to provide the plurality of control signals.

11. A radio-frequency (RF) apparatus, comprising:

a first integrated circuit, including:

an adjustable capacitor having a capacitance value adapted to be adjustable in response to a plurality of control signals;

a voltage generator configured to generate a measurement voltage that depends in part on the capacitance value of the adjustable capacitor; and

a controller configured to receive the measurement voltage and a reference voltage, the controller further configured to provide the plurality of control signals based on the relative values of the measurement voltage and the reference voltage.

12. The radio-frequency apparatus according to claim 11, wherein the measurement voltage is generated by alternately charging and discharging the adjustable capacitor.

13. The radio-frequency apparatus according to claim 12, wherein the adjustable capacitor comprises a plurality of switchable capacitors configured to adjust the capacitance value of the adjustable capacitor in response to the plurality of control signals.

14. The radio-frequency apparatus according to claim 13, further comprising analog-to-digital converter circuitry, wherein the adjustable capacitor resides within the analog-to-digital converter circuitry.

15. The radio-frequency apparatus according to claim 14, wherein the adjustable capacitor is calibrated by holding the plurality of control signals constant.

16. The radio-frequency apparatus according to claim 15, wherein the first integrated circuit further comprises radio-frequency receiver circuitry coupled to the analog-to-digital converter circuitry.

17. The radio-frequency apparatus according to claim 16, wherein the adjustable capacitor is calibrated after powering up the first integrated circuit.

18. The radio-frequency apparatus according to claim 17, wherein the adjustable capacitor is calibrated before a reception of a burst by the radio-frequency receiver circuitry.

19. The radio-frequency apparatus according to claim 18, further comprising a second integrated circuit coupled to the first integrated circuit, the second integrated circuit comprising digital signal processing circuitry configured to accept a digital output signal of the analog-to-digital converter circuitry.

20. The radio-frequency apparatus according to claim 15, wherein the plurality of switchable capacitors are coupled in parallel with one another.

21. The radio-frequency apparatus according to claim 20, wherein each switchable capacitor in the plurality of switchable capacitors comprises a capacitor coupled to a switch.

22. The radio-frequency apparatus according to claim 21, wherein each switch in the plurality of switchable capacitors responds to a respective signal in the plurality of control signals.

23. The radio-frequency apparatus according to claim 22, wherein the adjustable capacitor is charged in response to a first clock signal and discharged in response to a second clock signal, and wherein the first and second clock signals are non-overlapping.

24. The radio-frequency apparatus according to claim 23, wherein the adjustable capacitor further comprises a fixed capacitor coupled in parallel with the plurality of switchable capacitors.

25. The radio-frequency apparatus according to claim 24, wherein the controller comprises a finite-state machine configured to generate the plurality of control signals.

26. The radio-frequency apparatus according to claim 25, wherein the finite-state machine uses successive approximation to generate the plurality of control signals.

27. The radio-frequency apparatus according to claim 15, wherein the first integrated circuit further comprises radio-frequency receiver circuitry coupled to the analog-to-digital converter circuitry, the radio-frequency receiver circuitry comprising a cascade coupling of a low-noise amplifier and a mixer.

28. The radio-frequency apparatus according to claim 27, wherein the adjustable capacitor is calibrated after powering up the radio-frequency circuitry within the first integrated circuit.

29. The radio-frequency apparatus according to claim 28, wherein the adjustable capacitor is calibrated before a reception of a burst by the radio-frequency receiver circuitry.

30. The radio-frequency apparatus according to claim 29, further comprising a second integrated circuit coupled to the first integrated circuit, the second integrated circuit comprising digital signal processing circuitry configured to accept a digital output signal of the analog-to-digital converter circuitry.

31. A method of calibrating circuitry within a first integrated circuit, comprising:

adjusting a capacitance value of an adjustable capacitor included within the first integrated circuit, the capacitance value of the adjustable capacitor configured to be adjustable in response to a plurality of control signals;

generating a measurement voltage, a voltage value of the measurement voltage being dependent in part on the capacitance value of the adjustable capacitor;

supplying to the adjustable capacitor the plurality of control signals generated by a controller, the controller configured to receive the measurement voltage and a reference voltage and to provide the plurality of control signals based on the relative values of the measurement voltage and the reference voltage.

32. The method according to claim 31, wherein generating the measurement voltage further comprises alternately charging and discharging the adjustable capacitor.

33. The method according to claim 32, wherein adjusting the capacitance value of the adjustable capacitor comprises using a plurality of switchable capacitors configured to adjust the capacitance value of the adjustable capacitor in response to the plurality of control signals.

34. The method according to claim 33, wherein the adjustable capacitor is included in an analog-to-digital converter circuitry adapted to reside within the first integrated circuit.

35. The method according to claim 34, further comprising calibrating the adjustable capacitor by holding constant the plurality of control signals.

36. The method according to claim 35, wherein the plurality of switchable capacitors are coupled in parallel with one another, and wherein each switchable capacitor in the plurality of switchable capacitors comprises a capacitor coupled to a switch, and wherein each switch is configured to respond to a respective signal in the plurality of control signals.

37. The method according to claim 36, wherein generating the measurement voltage further comprises:

charging the adjustable capacitor in response to a first clock signal; and

discharging the adjustable capacitor in response to a second clock signal, wherein the first and second clock signals are non-overlapping.

38. The method according to claim 37, wherein the adjustable capacitor further comprises a fixed capacitor coupled in parallel with the plurality of switchable capacitors.

39. The method according to claim 38, further comprising providing within the controller a finite-state machine configured to generate the plurality of control signals by using successive approximation.

40. The method according to claim 39, further comprising receiving radio-frequency signals by using a radio-frequency receiver circuitry, the radio-frequency circuitry

included in the first integrated circuit and coupled to the analog-to-digital converter circuitry.

41. The method according to claim 40, further comprising calibrating the adjustable capacitor after powering up the first integrated circuit.

42. The method according to claim 41, further comprising calibrating the adjustable capacitor before a reception of a burst by the radio-frequency receiver circuitry.

43. The method according to claim 42, further comprising providing a second integrated circuit coupled to the first integrated circuit, the second integrated circuit comprising digital signal processing circuitry configured to accept a digital output signal of the analog-to-digital converter circuitry.